What is claimed is:

1. A semiconductor integrated circuit device having a plurality of word lines extending in a first direction, a plurality of bit lines extending in a second direction intersecting the first directions, and a plurality of memory cells each having a transistor and a capacitor placed on the bit line, said semiconductor integrated circuit device comprising:

active regions formed in a surface of a semiconductor substrate, intersecting adjacent first and second word lines among the plurality of word lines and a first bit line among the plurality of bit lines, extending in a third direction different from the first and the second direction and having a predetermined width along a fourth direction perpendicular to the third direction;

first and second semiconductor regions formed in the active regions and serving as sources and drains of the transistors;

first and second electrodes for the capacitors;

a dielectric film formed between the first and the second electrodes of the capacitors;

a first insulating film formed between the bit lines and the first electrodes; and

a first conducting layer having portions formed in first openings formed in the first insulating film and

electrically connecting the first or the second semiconductor regions to the first electrodes serving as lower electrodes of the capacitors;

wherein portions of the first conducting layer are arranged in regions surrounded by the word lines and the bit lines, respectively, and centers of the portions of the first conducting layer are dislocated from positions on center lines of the active regions extending in the third direction.

2. The semiconductor integrated circuit device according to claim 1 further comprising a second conducting layer formed between the first conducting layer and either of the first and the second semiconductor regions; wherein width of portions of the second conducting layer in the first direction is greater than that of portions of the first conducting layer.

3. The semiconductor integrated circuit device according to claim 2, wherein center distance with respect to the first direction between the adjacent portions of the second conducting layer is smaller than that between the adjacent portions of the first conducting layer overlying the second conducting layer.

4. The semiconductor integrated circuit device according to claim 2, wherein center distance with respect to the second direction between the adjacent portions of

the second conducting layer is greater than that between the adjacent portions of the first conducting layer overlying the second conducting layer.

5. The semiconductor integrated circuit device according to claim 2, wherein a silicon nitride film is formed between the word lines and the second conducting layer, and any silicon nitride film is not formed between the bit lines and the first conducting layer.

6. The semiconductor integrated circuit device according to claim 1, wherein width with respect to the second direction of portions of the first conducting layer is smaller than width of the word lines.

7. The semiconductor integrated circuit device according to claim 1, wherein width of the bit lines is smaller than that of the word lines.

8. A semiconductor integrated circuit device comprising:

adjacent first and second word lines extending in a first direction;

third word lines disposed adjacent to the first word lines opposite to the second word lines with respect to the first word lines;

fourth word lines disposed adjacent to the second word lines opposite to the first word lines with respect to the second word lines;

adjacent first, second and third bit lines extending in a second direction intersecting the first direction;

active regions extending in a third direction intersecting the first and the second directions;

first semiconductor regions formed in the active regions between the first and the second word lines;

second semiconductor regions formed in the active regions between the first and the third word lines and between the second and the fourth word lines;

first and second electrodes for forming capacitors;

a dielectric film formed between the first and the second electrodes; and

a plurality of first conducting layers having portions electrically connecting the second semiconductor regions to the first electrodes;

wherein the portions of the first conducting layers are formed in regions surrounded by the word lines and the bit lines, respectively, an angle between a straight line connecting a center of each portion of the first conducting layer disposed between the first and the third word lines to a center of each portions of the first conducting layer disposed between the second and the fourth word lines and the first direction is smaller than an angle between the third direction and the first direction.

9. A semiconductor integrated circuit device having

a plurality of word lines extending in a first direction, a plurality of bit lines extending in a second direction intersecting the first direction, and a plurality of memory cells each including a transistor and a capacitor disposed on the bit line, said semiconductor integrated circuit device comprising:

active regions formed on a semiconductor substrate, extending in a third direction different from the first and the second directions and each intersecting the two word lines and the one bit line;

first and second semiconductor regions formed in the active regions and serving as sources and drains of the transistors;

first and second electrodes for forming the capacitors;

a dielectric film formed between the first and the second electrodes;

a first insulating film formed between the bit lines and the first electrodes; and

a first conducting layer having portions formed in first openings formed in the first insulating film and electrically connecting either of the first and the second semiconductor regions to the first electrodes;

wherein portions of the first conducting layer are arranged in regions surrounded by the word lines and the

bit lines, respectively, and the portions of the first conducting layer has a width in the second direction smaller than that of the word lines.

10. The semiconductor integrated circuit device according to claim 9 further comprising a second conducting layer formed between the first conducting layer and either of the first and the second semiconductor regions, wherein width with respect to the first direction of portions of the second conducting layer is greater than that of the portions of the first conducting layer.

11. The semiconductor integrated circuit device according to 10, wherein center distance with respect to the first direction between the adjacent portions of the second conducting layer is smaller than that between the adjacent portions of the first conducting layer overlying the second conducting layer.

12. The semiconductor integrated circuit device according to claim 10, wherein center distance with respect to the second direction between the adjacent portions of the second conducting layer is greater than that between the adjacent portions of the first conducting layer overlying the second conducting layer.

13. The semiconductor integrated circuit device according to claim 10, wherein a silicon nitride film is formed between the word lines and the second conducting

layer, and any silicon nitride film is not formed between the bit lines and the first conducting layer.

14. The semiconductor integrated circuit device according to claim 9, wherein width of the bit lines is smaller than that of the word lines.

15. A semiconductor integrated circuit device having a plurality of word lines extending in a first direction, a plurality of bit lines extending in a second direction intersecting the first direction, and a plurality of memory cells each including a transistor and a capacitor disposed on the bit line, said semiconductor integrated circuit device comprising:

first and second electrodes for forming the capacitors formed on a semiconductor substrate;

a dielectric film formed between the first and the second electrodes;

a first insulating film formed between the bit lines and the first electrodes; and

a first conducting layer having portions formed in first openings formed in the first insulating film and electrically connecting the transistors to the first electrodes;

wherein portions of the first conducting layer are arranged in regions surrounded by the word lines and the bit lines, respectively, and the bit lines have a width

smaller than that of the word lines.

16. The semiconductor integrated circuit device according to claim 15 further comprising a second conducting layer formed between the first conducting layer and either of the first and the second semiconductor regions, wherein width with respect to the first direction of portions of the second conducting layer is greater than that of the portions of the first conducting layer.

17. The semiconductor integrated circuit device according to 16, wherein center distance with respect to the first direction between the adjacent portions of the second conducting layer is smaller than that between the adjacent portions of the first conducting layer overlying the second conducting layer.

18. The semiconductor integrated circuit device according to claim 16, wherein center distance with respect to the second direction between the adjacent portions of the second conducting layer is greater than that between the adjacent portions of the first conducting layer overlying the second conducting layer.

19. The semiconductor integrated circuit device according to claim 16, wherein a silicon nitride film is formed between the word lines and the second conducting layer, and any silicon nitride film is not formed between the bit lines and the first conducting layer.

20. A semiconductor integrated circuit device fabricating method, comprising the steps of:

adjacently forming first, second and third conducting layers on a semiconductor substrate;

forming a first insulating film over the upper surfaces and side walls of the first, the second and the third conducting layers;

forming a second insulating film over the first insulating film so as to fill up gaps between the first, the second and the third conducting layers;

forming first openings in the first and the second insulating films so that portions of a surface of the semiconductor substrate between the first and the second conducting layers are exposed;

forming a fourth conducting layer so as to fill up the first openings;

forming second openings in the first and the second insulating films so that portions of the surface of the semiconductor substrate between the second and the third conducting layers are exposed; and

forming a fifth conducting layer so as to fill up the second openings.

21. The semiconductor integrated circuit device fabricating method according to claim 20 further comprising the steps of:

forming a third insulating film over the fifth conducting layer and forming third openings in the third insulating film so that portions of the surface of the fifth conducting layer are exposed;

forming a sixth insulating film so as to fill up the third openings, subjecting the sixth insulating film to anisotropic etching to form side wall insulating films on side walls of the third openings; and

forming a sixth conducting layer so as to fill up the third openings.

22. A semiconductor integrated circuit device fabricating method, comprising the steps of:

forming first and second conducting layers in a memory cell forming regions on a semiconductor substrate and forming a third conducting layer in a peripheral circuit forming region on the semiconductor substrate;

forming a first insulating film over the first, the second and the third conducting layers in a thickness such that a gap between the first and the second conducting layers is not filled up;

forming a second insulating film over the first, the second and the third conducting layers in a thickness such that the gap between the first and the second conducting layers is filled up;

forming a third insulating film over the memory cell

forming region; and

forming a side wall insulating film over side walls of the third conducting layer by subjecting portions of the first and the second insulating films formed over the third conducting layer to anisotropic etching.

23. The semiconductor integrated circuit device fabricating method according to claim 22 further comprising the steps of:

forming a fourth insulating film over a portion of the second insulating film corresponding to the memory cell forming region; and

etching the first, the second and the fourth insulting films to form openings between the first and the second conducting layers;

wherein the first insulating film is a silicon nitride film, and the second and the fourth insulating films are silicon oxide film.